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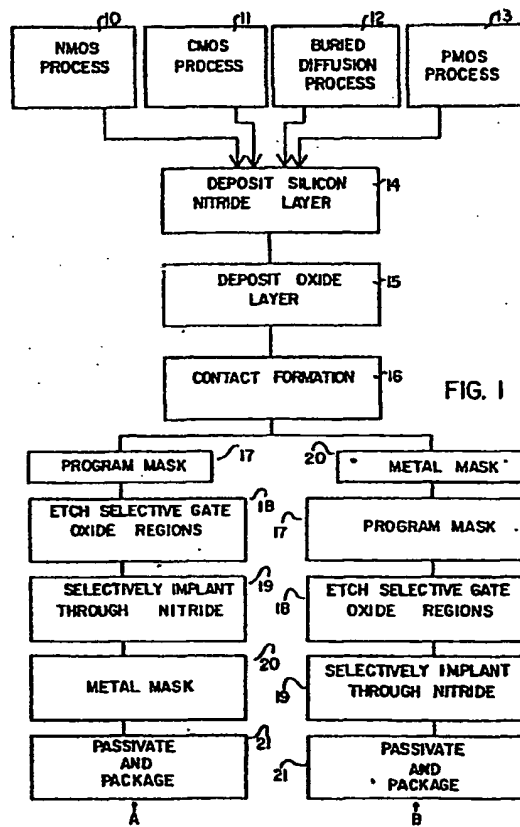
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(54) **Process of producing custom programmed read only memory.**

(57) A late mask programming process is provided for factory programmed ROMs or logic circuitry. MOS transistors functioning as ROM cells or in logic circuitry are fabricated by a standard MOS Process. Then, a thin stop layer of silicon nitride is provided over the transistors and followed by a layer of silicon dioxide. Programming is accomplished by applying a program mask and etching through the layers overlying the gate regions of selected transistors down to the silicon nitride stop layer. The silicon nitride stop layer prevents overetching and shorting of the gates. Then, ions are implanted underneath the gates of the selected MOS transistors to alter their threshold so, for example, as ROM cells they signify a different state than those cells whose transistor gates are not implanted with ions. The silicon nitride layer serves to stop the etch solution but permits the ions to pass through, penetrate the substrate and raise the thresholds of the selected transistors. The silicon dioxide layer stops the ions from being implanted into the nonselected transistors.

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5 PROCESS OF PRODUCING CUSTOM PROGRAMMED READ ONLY MEMORY
6 DESCRIPTION

7 This invention relates to a process of producing a
8 custom programmed read only memory (ROM).

9 In the semiconductor industry the fabrication of
10 devices has progressed from discrete devices to devices
11 integrating multiple devices on the same chip. Such
12 integrated devices have progressed from small scale inte-
13 gration, to medium scale integration, to large scale
14 integration and now to very large scale integration.
15 These integrated devices typically have been designed by
16 semiconductor manufacturers with the view to satisfying
17 the requirements of a broad range of customers. Such
18 customers could pick and choose from the offerings of all
19 domestic and foreign commercial suppliers of standard
20 semiconductor devices. For many applications, however,
21 standard devices of this type have not been available to
22 optimally meet the requirements of the particular appli-
23 cation. For extremely high volume applications, large
24 companies have been able to custom order parts or, in some
25 cases, have set up in-house fabrication facilities to
26 produce their own semiconductor devices to their own
27 specifications. Small companies or low volume applications
28 have not been able to advantageously utilize such custom
29 fabrication. More recently, a number of companies have
30 offered custom semiconductor devices based on so-called
31 gate arrays which are alterable during various stages of
32 the fabrication process in accordance with the design of
33 the customer. These so-called silicon foundries are
34 believed to provide a satisfactory answer to the system
35 requirements of many users, particularly low-volume users.
36 However, it is imperative that they do not introduce
37 delays into the system design and development cycle.

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1 In addition to the logic arrangements of gate arrays,
2 programmable memory arrays such as read only memories
3 (ROMs) are now in widespread use. The memory patterns in
4 ROMs may also be fixed at the factory to reflect initial
5 or reference data provided by the customer or may be
6 programmed in the field by fusing links or by electrically
7 programming EPROMs. In programming ROMs at the factory
8 the requirement has been the relatively straightforward
9 one of programming a predetermined pattern into the avail-
10 able cells of the memory during fabrication. The manufac-
11 turer of ROMs, by some means, incorporates into its process
12 a bit map provided by the customer which will determine
13 the state (ones or zeros) of each bit in the ROM.

14 In the programming of ROMs at the factory, the conven-
15 tional approaches have involved process steps at intermed-
16 iate stages of the process sequence. Thus, once a customer
17 has placed an order, it has always been necessary to carry
18 out the programming step and then complete the processing
19 of the wafers through all the rest of the processing
20 steps. This necessity has resulted in significant turn-
21 around time from customer order to availability of prototype.
22 The standard ROM fabrication technologies have required
23 that the ROM cell, a single MOS transistor, be programmed
24 to its zero-logic state by various techniques, techniques
25 which have occurred early in the process sequence or which
26 have unduly enlarged the cell size. For example, the
27 oxide is sometimes made thicker under certain ones of the
28 transistors, thereby increasing the threshold voltage of
29 the transistor. Or, in the contact mask, the zero-state
30 may be obtained by not making contacts to those gates
31 requiring a zero-state. And in one process gates are not
32 formed over selected prospective MOS transistors. See C.
33 K. Kuo, "Method of Making a Metal Programmable MOS Read
34 Only Memory Device," U.S. Patent No. 4,384,399; see also
35 the references and discussion therein. In some processes
36 the zero-state is programmed in the metal mask by not
37 making an electrical connection with the gate and in still
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other processes the sources or drains are offset from the gate for selected transistors which are to have a zero state; see R.S. Countryman, et al., "Method of Programming ROM by Offset Masking of Selected gates," U.S. Patent No. 4,380,866. See, e.g., C.K. Kuo, "Post-Metal Programmable MOS Read Only Memory", U.S. Patent No. 4,390,971. And in still other MOS processes, the programming of ROM cells occurs by implanting ions through polysilicon layers in selected transistors to increase the threshold to render them nonconductive and produce the zero state. With all of the above programming techniques, the programming occurs while the devices are being defined or a penalty of increased cell size is incurred.

The invention accordingly provides a process of producing a custom programmed read-only memory (ROM) in a silicon wafer, the process comprising the steps of:

- fabricating an array of metal oxide silicon (MOS) transistors in a silicon wafer up to the stage of contact formation;
- depositing a layer of silicon nitride over the transistors;
- depositing a layer of silicon dioxide over the layer of silicon nitride;
- applying to the wafer a program mask containing a pattern which represents a map of selected transistors in the array of transistors of which the threshold voltages are to be altered whereby the gate regions above the selected transistors are exposed;
- etching the layers of silicon dioxide above the selected gate regions down to the silicon nitride layer; and
- implanting ions through the silicon nitride layer into the silicon regions underneath the gates to alter the threshold voltages of the selected transistors, the silicon dioxide layer serving to stop the passage of the ions.

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Definition of contacts to active device regions can precede the etching through the layers overlying the gate regions of the selected transistors down to the silicon nitride layer, which prevents over-etching and shorting of the gates of the selected transistors, by stopping the etch solution but permits the ions to pass through to penetrate the substate. Alternatively, the programming and all subsequent steps are accomplished after the metal mask step.

The present invention can thus provide a process of producing ROMs wherein ROM programming occurs late in the process. The process does not add to cell size.

For a more complete understanding of the present invention, reference may be had to the following illustrative description and accompanying drawings, in which:

Figure 1 is a block diagram showing alternative fabrication technologies which may use at the end of the process sequence, a process in accordance with the present invention; and

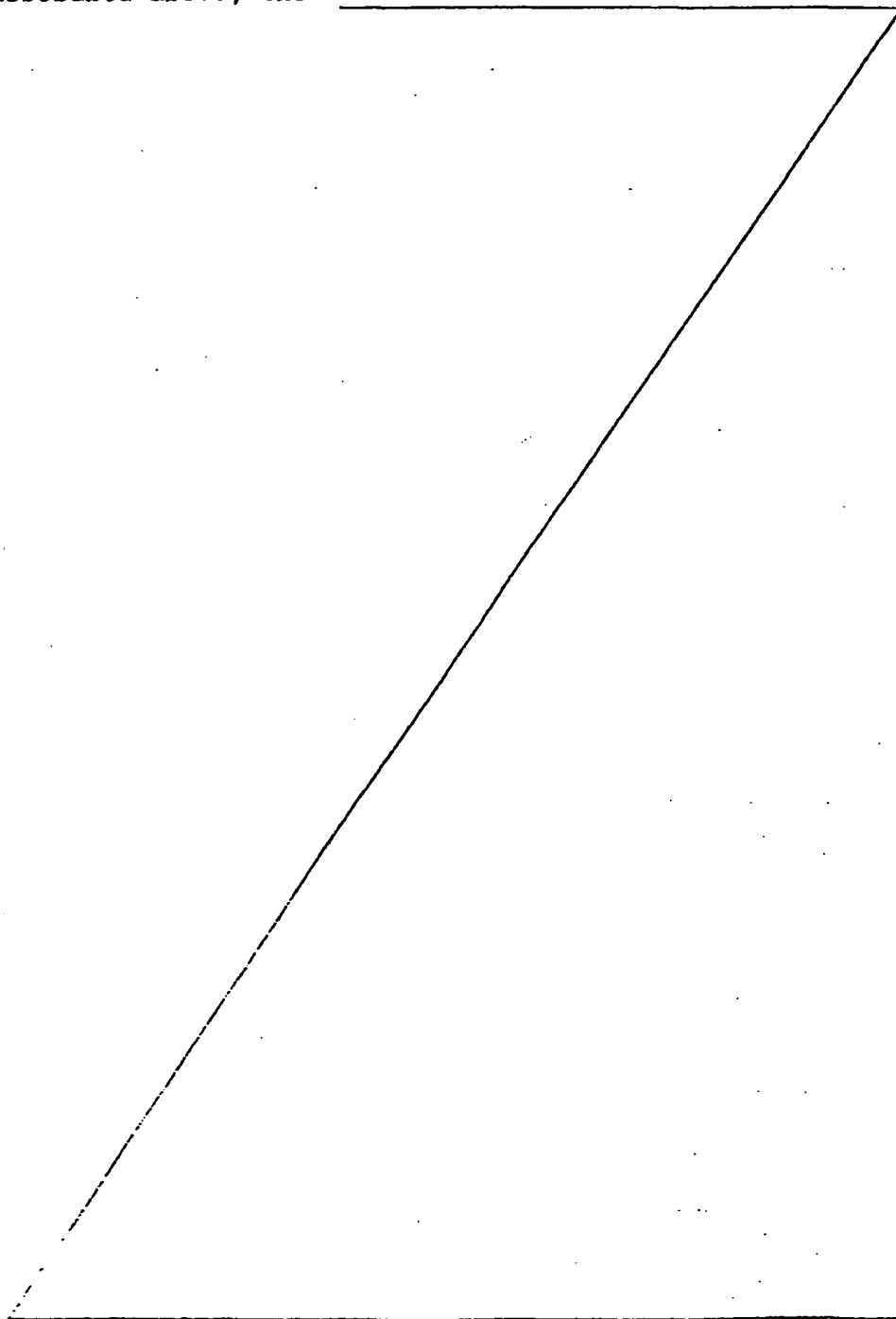
Figures 2a-21 are a series of cross-sectional views of an MOS transistor being formed by an NMOS process (Figs. 2a-2g) and then being programmed (Figs. 2h-21) in accordance with a process in accordance with the present invention.

In producing custom integrated circuits, the overall process typically has four major stages. The diffusion or implantation stage defines and produces those areas such as sources or drains that are to serve as active electrical regions. The metal layer design stage interconnects the active electrical regions by conductive lines of metal or doped polysilicon to interconnect individual transistors (or cells) into logic or memory arrangements. The wafer personalization stage is where, in accordance with a customer's design, particular logic building blocks are selected and interconnected or where,

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if not previously accomplished, ROM cells are programmed in accordance with the bit map of a customer. Then, in the final stage the device is packaged and tested. As described above, the



1 conventional approach to programming ROM cells is to carry
2 out the programming in stages 1 to 3 and typically early
3 in the overall process sequence. With the several tech-
4 niques described above which occur late in the process
5 sequence, a penalty in increased cell size is incurred.

6 As described previously, the conventional techniques
7 for factory programming ROMs often include process steps
8 which are carried out early in the process sequence. For
9 example, the programming of the field oxide by providing
10 thick oxide underneath certain transistors occurs as early
11 as the field oxide definition step shown in Figure 2c.
12 The omission of a gate over a particular prospective
13 transistor could occur as early as step 2f. Selectively
14 contacting the gates is a programming technique which
15 occurs in the process at about the steps indicated in Fig.
16 2j, and, the omission of a metal interconnect through the
17 metal mask occurs at about the step indicated in Fig. 2k.
18 Either these steps occur relatively early in the process
19 sequence or they result in a bigger cell size. Ideally,
20 for the fast turnaround of a ROM to be custom programmed,
21 a custom IC company would have wafers on the fully pro-
22 cessed to the point of programming. With the late mask
23 programming technique of the present invention, the setting
24 of the state of a particular MOS transistor or ROM cell
25 does not occur until the stage of the process indicated by
26 Figure 2k. Cell size is not increased; only the threshold
27 level of selected cells is altered. Wafers can be stored
28 with all processing completed up to the stage of Figure 2k
29 and then rapidly completed with the last several steps up
30 to final packaging. This permits extremely fast turnaround
31 for customers once they supply a bit map for programming
32 of custom ROMs. Turnaround time can thus be measured in
33 two to three days rather than in two to three weeks.

34 The process sequences for various embodiments of the
35 present invention in the context of programming ROMs may
36 be seen in the block diagram of Figure 1. Any conventional
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1 MOS process for ROMs may be utilized to define the indi-
2 vidual transistors. Thus, NMOS process 10, CMOS process 11,
3 buried diffusion process 12 or PMOS process 13 may be
4 utilized up to the stage of definition of the transistors.
5 At this time in the personalization, a stop layer of
6 silicon nitride is applied in step 14. This thin layer of
7 about 100 angstroms to about 1000 angstroms serves later
8 to prevent over-etching of the oxide in selective etch
9 step 18, as described in detail subsequently. Next, an
10 oxide layer is applied by conventional vapor deposition
11 techniques to a thickness of approximately 10,000Å. Then
12 the contacts are formed in step 16 to the individual
13 sources and drains and to the poly interconnects and to
14 gates. In embodiment A at this late time in processing a
15 program mask with the bit map for programming the ROM is
16 applied in step 17 to open up the oxide above the gates of
17 those MOS transistors which are to be programmed to the
18 zero state. The oxide above the gates of these transistors
19 is etched in step 18, down to the thin silicon nitride
20 layer applied previously in step 14. Preferably, an etch
21 is used which preferentially etches silicon dioxide over
22 silicon nitride. The thin nitride layer, as described in
23 detail subsequently, prevents over-etching so that there
24 is no shorting of the gates to the source, drain or sub-
25 strate regions. Then an ion implantation step 19 is
26 carried out to raise the thresholds of those MOS transis-
27 tors whose gates are exposed. The oxide remaining over
28 the gates of the other MOS transistors prevents them from
29 being affected during the ion implantation. The devices
30 are then processed through standard processing techniques
31 including metal evaporation and metal masking in step 20
32 and passivating and packaging in step 21. In embodiment B
33 the metal evaporation and metal mask step 20 is carried
34 out immediately after contact formation step 16. Thereafter,
35 the program mask with the bit map for programming the ROM
36 is applied in step 17 to open up the oxide above the gates
37 of those MOS transistors which are to be programmed to the
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1 zero state. The oxide above the gates of these transis-
2 tors is then etched in step 18, down to the thin silicon
3 nitride layer applied previously in step 14. In embodi-
4 ment B, the thin nitride layer, as with embodiment A,
5 prevents overetching so that there is no shorting of the
6 gates to the source, drain or substrate regions. Then the
7 ion implantation step 19 is carried out to raise the
8 thresholds of those MOS transistors whose gates are exposed.
9 The oxide remaining over the gates of the other MOS tran-
10 sistors prevents them from being affected during the ion
11 implanatation. The devices are then passivated and packaged
12 in step 21.

13 To fully examine the process sequence of embodiment A
14 of the present invention and to particularly point out the
15 stages at which programming is done in the prior art as
16 compared with the process of the present invention, refer-
17 ence should be made to the process sequence shown in Figs.
18 2a-21. As discussed above, the portions of this specific
19 process through definition of the transistors may vary
20 with other embodiments but will remain the same for the
21 application of the stop layer of silicon nitride and the
22 programming steps. The process sequence shown for defining
23 the transistors is an NMOS process. In Fig. 2a, a silicon
24 wafer 24 has a thin layer 26 of thermal oxide grown on its
25 surface. A 700Å layer of silicon nitride 25 is deposited
26 on the surface of silicon oxide 26. In Figure 2b the
27 lateral expanse of a single MOS transistor is shown under-
28 neath resist region 27 and between field oxide areas to be
29 formed. The transistor is exemplary of each transistor in
30 a standard read-only memory array. The nitride layer 25
31 is etched everywhere except under the resist. Subsequently,
32 a field implant 28 of 5×10^{12} atoms per square centimeter
33 is introduced into the silicon substrate 24 through the
34 exposed oxide layer 25 at an implantation energy of 100
35 kilovolts. Field oxide 29 is then thermally grown as
36 shown in Fig. 2c. The field implant 28 is slightly dif-
37 fused outwardly as a result of the high-temperature process.
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1 An implantation of boron at 4×10^{11} atoms per square centi-
2 meter is carried out at an implantation energy of 50
3 kilovolts as shown in Fig. 2d to produce the gate implant
4 region 19 and to provide the threshold voltage of the
5 gate, typically about one volt. The implantation levels
6 will vary as device requirements dictate. In a preferred
7 embodiment before the gate implant is carried out, the
8 initial oxide and nitride layers are stripped and a thin
9 gate oxide is intentionally grown. Next, as shown in
10 Fig. 2e, a section 31 of the surface of the silicon
11 wafer 24 is opened up above the drain source region to be
12 formed. The oxide is removed by chemical or dry plasma
13 etching while a poly contact mask is in place. A layer 30
14 of highly doped polycrystalline silicon is then applied to
15 contact the drain region to be formed. The polysilicon is
16 defined in Fig. 2f to leave a gate region 32 and an inter-
17 connection 33 which makes electrical contact with the
18 drain region 35 which has not been formed.

19 The final step in the definition of the MOS transistor
20 is accomplished by the implantation shown in Fig. 2g. In
21 this embodiment, 8×10^{15} atoms per square centimeter of
22 arsenic is implanted at an implantation energy of 75
23 kilovolts. These ions are driven through the thin oxide
24 over the source region 34 and are also driven into a drain
25 region 35. In order to drive the arsenic further into the
26 silicon substrate 24, a high-temperature thermal drive-in
27 diffusion is carried out at a temperature on the order of
28 1050°C for about 15-20 minutes. This thermal drive-in
29 produces source region 34' and drain region 35'. As a
30 consequence of the thermal drive-in, the field oxide 29 is
31 slightly increased in size and oxide layer 40 grows over
32 gate 32 and over the exposed surface of drain region 35',
33 source region 34', and polysilicon interconnect 33. This
34 oxide region 40 will remain over the gate for the duration
35 of processing. The MOS transistor illustrated in this
36 process sequence is now fully formed and would be opera-
37 tional upon the application of gate, source and drain
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1 contacts and the application of appropriate signals. It
2 is at this late stage in the process sequence that the
3 setting of the transistor to a zero state is accomplished.
4 In accordance with the process of the present invention, a
5 very thin layer 34 of silicon nitride is then applied to
6 the entire surface. Preferably, this layer has a thickness
7 of 100-1000Å. The layer is thick enough to prevent over-
8 etching by an etch which preferentially etches silicon
9 dioxide over silicon nitride, such as dilute hydrofluoric
10 acide, but is thin enough to permit ions to be implanted
11 therethrough as described subsequently. Thereafter, as
12 shown in Fig. 2i, a layer 36 of deposited oxide (called
13 PVX) is applied over the entire structure. Typically,
14 this will be deposited by chemical vapor deposition and
15 have a thickness of about 10,000Å. The PVX serves to
16 insulate underlying layers from overlying metal lines and
17 stops ions from being implanted into transistors whose
18 thresholds are not to be altered. As shown in Figure 2j,
19 a contact mask is now used to open up access to the source
20 34', the drain 35', the polysilicon 33 and all other
21 regions to which electrical contacts are to be made. The
22 wafers are then processed through source and drain metal-
23 lization to define interconnects to sources, drains, gates
24 and polysilicon lines. Note defined interconnects 37 and
25 38 in Fig. 2k.

26 Up to this point in processing, no programming of ROM
27 cells has occurred. Any logic transistors on the chip
28 have been formed and indiscriminately interconnected and
29 all ROM cells are formed and potentially operational.
30 Subsequently, by programming, the transistors are rendered
31 disfunctional in certain ROM cells or in certain portions
32 of the logic circuitry by raising their thresholds so
33 high, typically higher than 5 volts, so that they are will
34 not function in the normal operation of the circuit. When
35 a particular customer provides a bit map or specifies
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1 logic circuitry, stored wafers may be taken out and pro-
2 cessed in accordance with the bit map or circuit logic.
3 The setting of an individual MOS transistor to a zero
4 state is accomplished by masking the PVX oxide in accordance
5 with the bit map as layed out on a program mask (step 17
6 in Fig. 1) and then etching through the PVX oxide down to
7 the silicon nitride stop layer. Then, in one embodiment,
8 to increase the thresholds of the selected transistors
9 approximately 25×10^{13} atoms of boron per square centimeter
10 is implanted at an energy of about 170 kilovolts. In
11 another embodiment a species of opposite conductivity type
12 is implanted to lower the threshold. What is required is
13 that one set of transistors have one threshold level and
14 another set have a different threshold level with the two
15 levels being sufficiently separated to permit reliable
16 differential detection.

17 In accordance with the process of present invention,
18 the presence of silicon nitride layer 34 has allowed the
19 etching over the selected gate regions to occur without
20 over-etching and shorting of the gate to the source or
21 drain regions or to the substrate. The silicon nitride
22 acts as an etch stop once the etch has penetrated the
23 overlying PVX and hence the etchant will not reach and
24 attack the underlying layers. In other processes where
25 implantation is used to alter threshold levels, without
26 the presence of the nitride layer 34, any attempt to open
27 up the areas of the gate region for implantation would
28 have potentially resulted in the shorting of the gate.
29 The implanted ions pass through the opened up region of
30 the thin nitride layer, penetrates the gate region and
31 enter the silicon under the gate to thereby raise the
32 threshold to above five volts. The ions are stopped by
33 the PVX elsewhere. In accordance with the preferred
34 embodiment of the process of this invention, this program-
35 ming occurs after contact formation (step 16, Fig. 1).
36 After this late process step the ROM array is now fully
37 programmed so that only a few steps yet remain such as
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1 passivation, pad mask, scribing and packaging of the
2 completed custom ROM; if logic circuitry is also on-board,
3 the logic pattern will also have been established by
4 raising the thresholds of selected transistors and effec-
5 tively removing them from the circuits. After the program-
6 ming, a passivating layer of silicon nitride 39 is applied
7 over the whole surface. The integrated circuits containing
8 the individual ROMs of Fig. 22 are then scribed and packaged
9 and provided to the customer. The completed integrated
10 circuit will contain certain ROM cells which are operational
11 transistors and other ROM cells whose threshold have been
12 raised and are effectively disfunctional in normal operation.

13 In embodiment B of Figure 1, each of the individual
14 steps of metal mask 20, program mask 17, selective gate
15 etch 18, selective implant 19 and passivate and package 21
16 are carried out as described above for embodiment A. The
17 program mask step 17 is carried out one step later than in
18 embodiment A thereby permitting the metal mask step 20 to
19 be carried out earlier in the process and slightly short-
20 ening the turnaround time from receipt of the customer's
21 map to availability of prototype. The presence of the
22 silicon nitride stop etch layer applied by step 14 is the
23 key in both embodiments B and A to allowing the implantation
24 step to be used effectively so late in the processing
25 sequence.

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CLAIMS

1. A process of producing a custom programmed read-only memory (ROM) in a silicon wafer, the process comprising the steps of:

- 5 fabricating an array of metal oxide silicon (MOS) transistors in a silicon wafer up to the stage of contact formation;
 depositing a layer of silicon nitride over the transistors;
10 depositing a layer of silicon dioxide over the layer of silicon nitride;
 applying to the wafer a program mask containing a pattern which represents a map of selected transistors in the array of transistors
15 of which the threshold voltages are to be altered whereby the gate regions above the selected transistors are exposed;
 etching the layers of silicon dioxide above the selected gate regions down to the silicon nitride layer; and
20 implanting ions through the silicon nitride layer into the silicon regions underneath the gates to alter the threshold voltages of the selected transistors, the silicon dioxide layer
25 serving to stop the passage of the ions.

2. A process as claimed in claim 1 wherein the threshold voltages of the selected transistors are lowered by the step of implanting ions.

3. A process as claimed in claim 1 wherein the
30 threshold voltages of the selected transistors are raised by the step of implanting ions.

4. A process as claimed in claim 1, 2 or 3 wherein the array of MOS transistors is fabricated by a NMOS process.

35 5. A process as claimed in claim 1, 2 or 3 wherein the array of MOS transistors is fabricated by

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a CMOS process.

6. A process as claimed in claim 1, 2 or 3 wherein the array of MOS transistors is fabricated by a buried diffusion process.

5 7. A process as claimed in claim 1, 2 or 3 wherein the array of MOS transistors is by a PMOS process.

8. A process as claimed in any preceding claim wherein each selected transistor of the MOS transistors comprises a ROM cell.

10 9. A process as claimed in any one of claims 1 to 7 wherein at least one of the selected transistors of the array of MOS transistors is incorporated in a logic circuit.

15 10. A process as claimed in any preceding claim wherein the layer of silicon nitride is deposited in a thickness in the range of 100Å to 1000 Å.

11. A process as claimed in any preceding claim wherein the layer of silicon dioxide is deposited in a thickness in the range of about 7,000 Å to about
20 10,000 Å.

12. A process as claimed in any preceding claim wherein contacts to the active regions in the transistors are formed through the silicon nitride layer after the step of depositing a layer of silicon dioxide.

25 13. A process as claimed in any preceding claim having, after the step of implanting ions, the steps of:

applying a metal mask to the wafer and forming metal interconnections between previously defined contacts to active device regions; and

30 applying a layer of passivating material to the wafer.

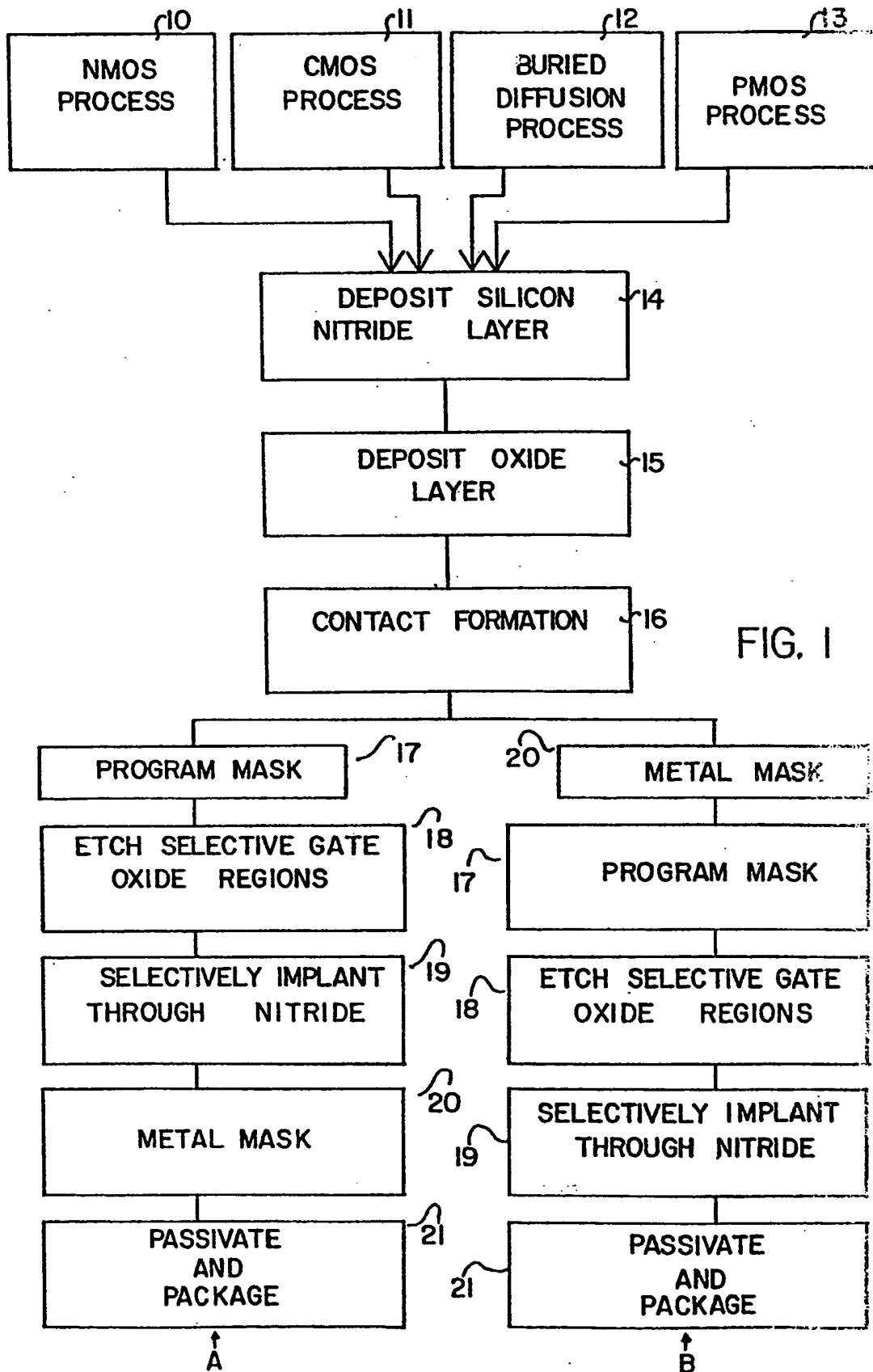
14. A process as claimed in any one of claims 1 to 11 having, before the step of applying a program mask to the wafer and after the step of depositing a layer of
35 silicon dioxide, the steps of:

forming contacts to the active regions in the transistors through the silicon nitride; and

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applying a mask to the wafer and forming
metal interconnections between the contacts to
the active regions.



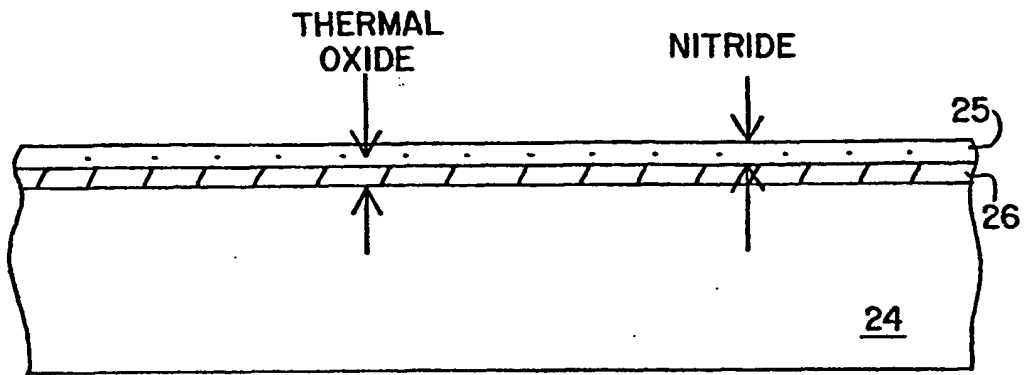


FIG. 2a

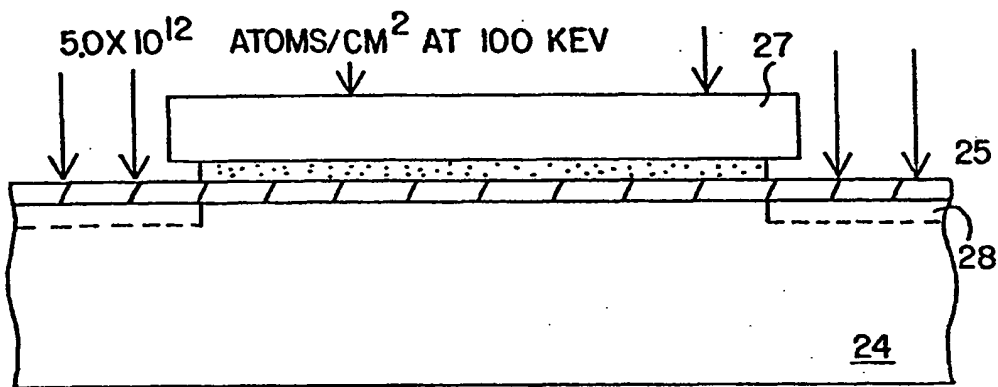


FIG. 2b

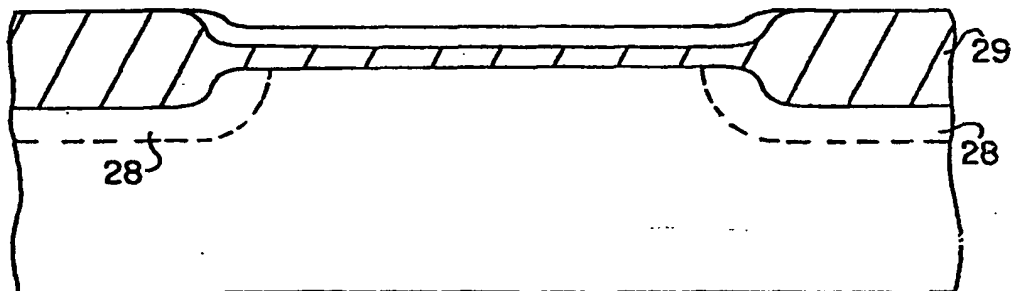


FIG. 2c

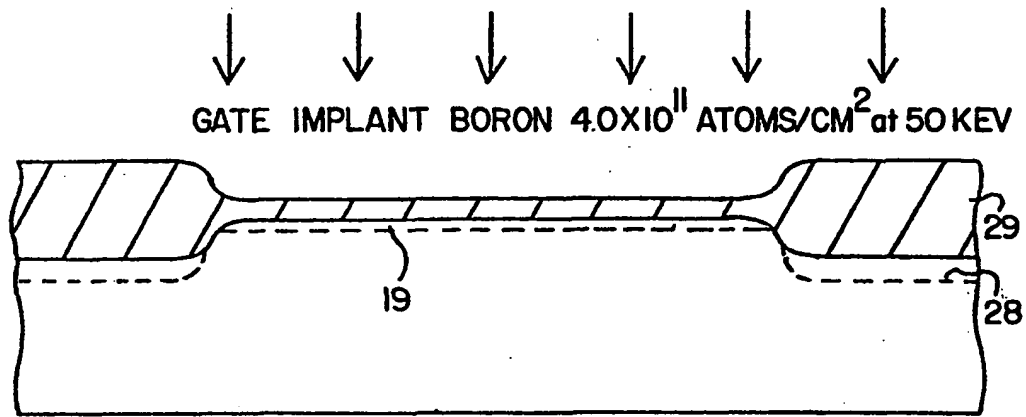


FIG. 2d

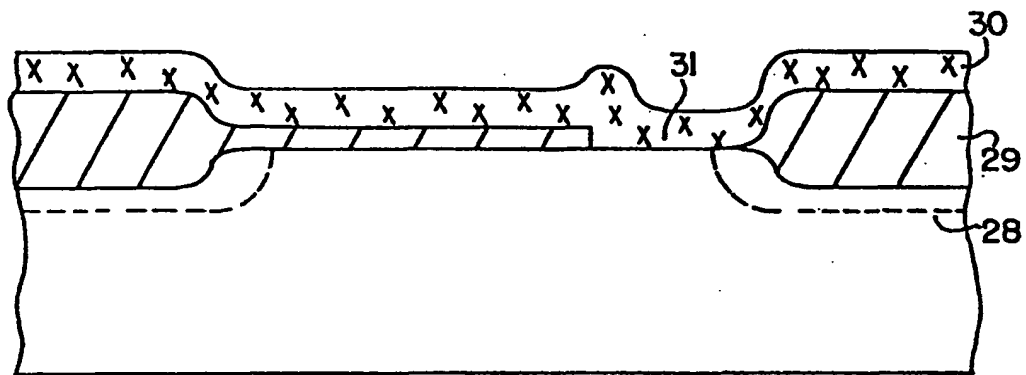


FIG. 2e

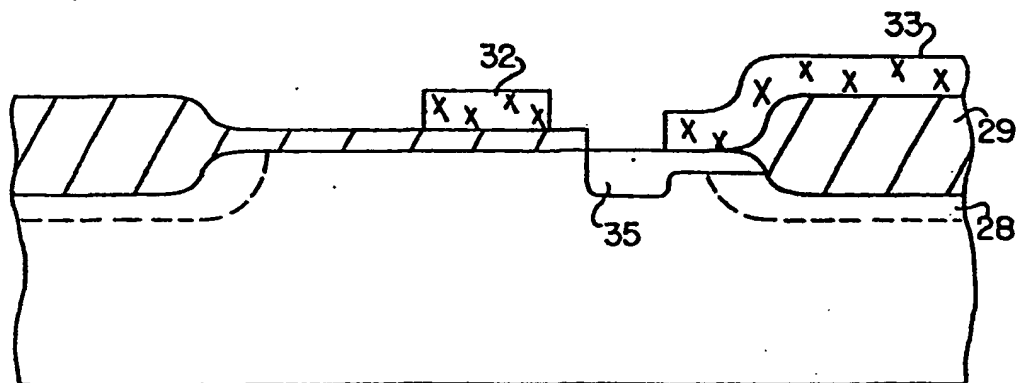


FIG. 2f

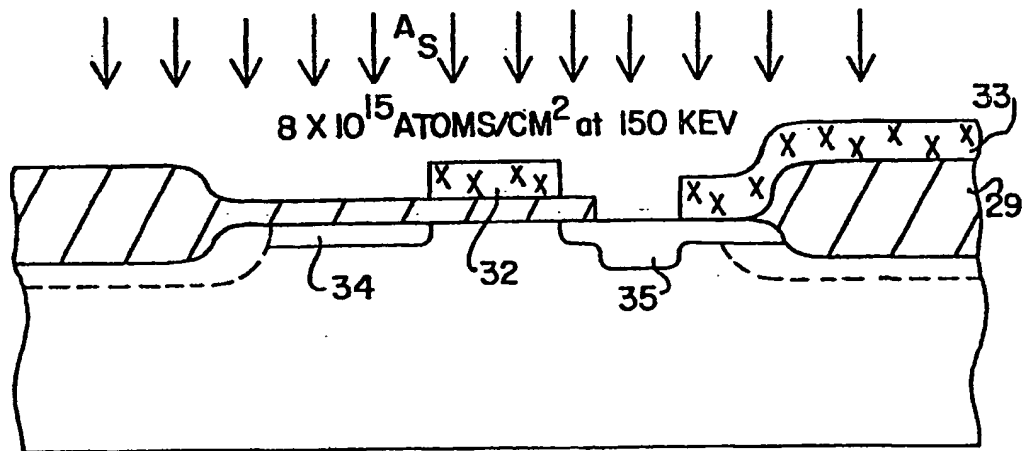


FIG. 2g

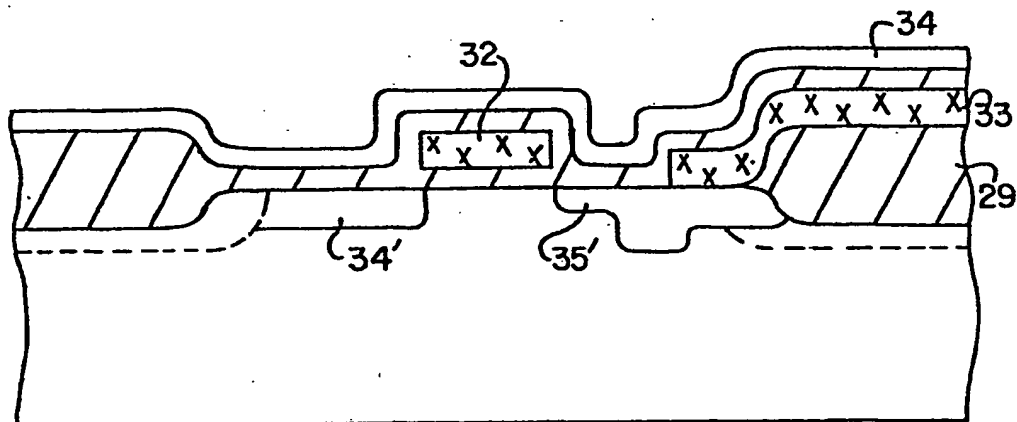


FIG. 2h

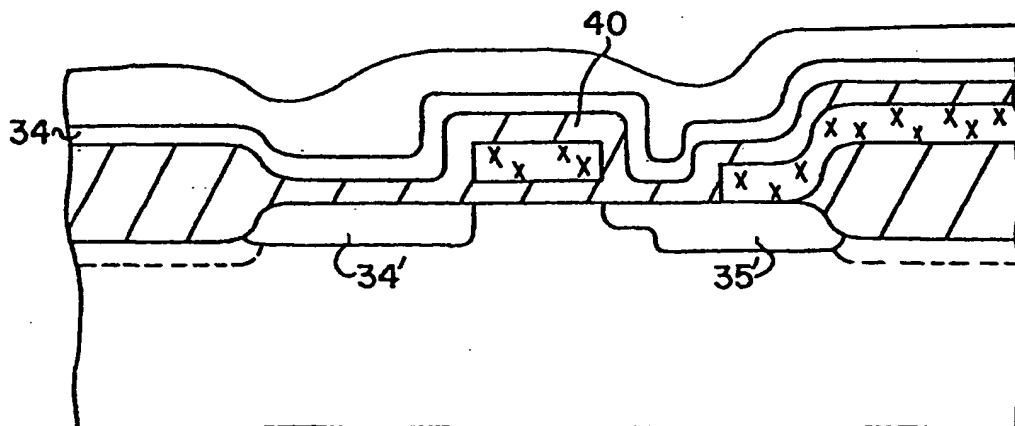


FIG. 2i

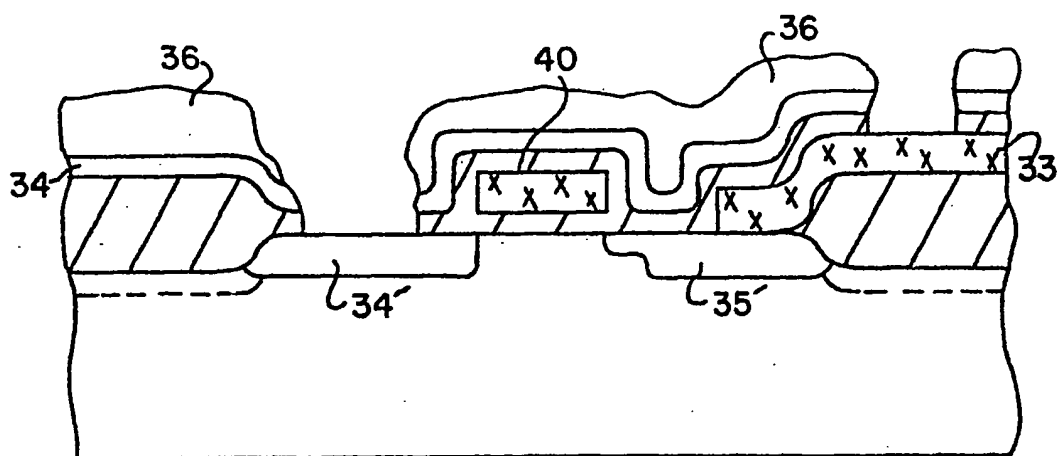


FIG. 2j

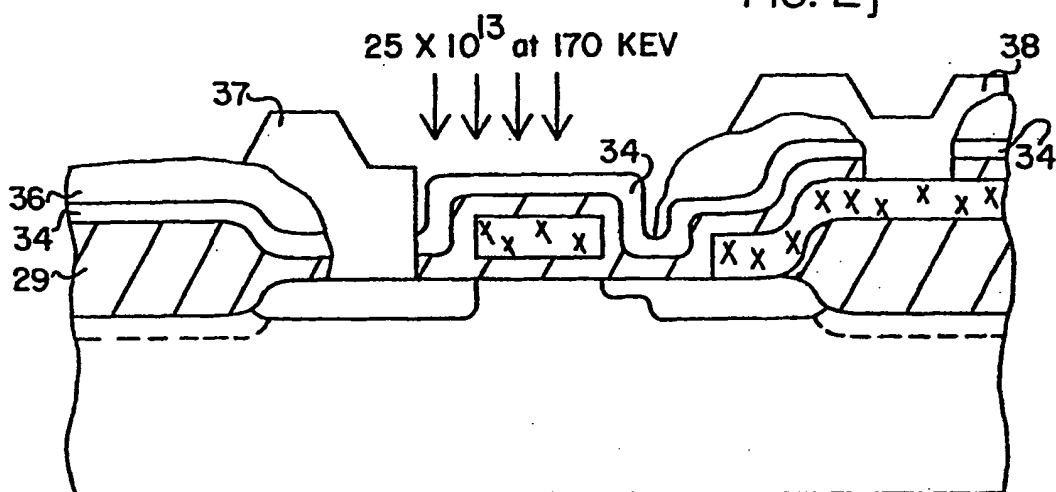


FIG. 2k

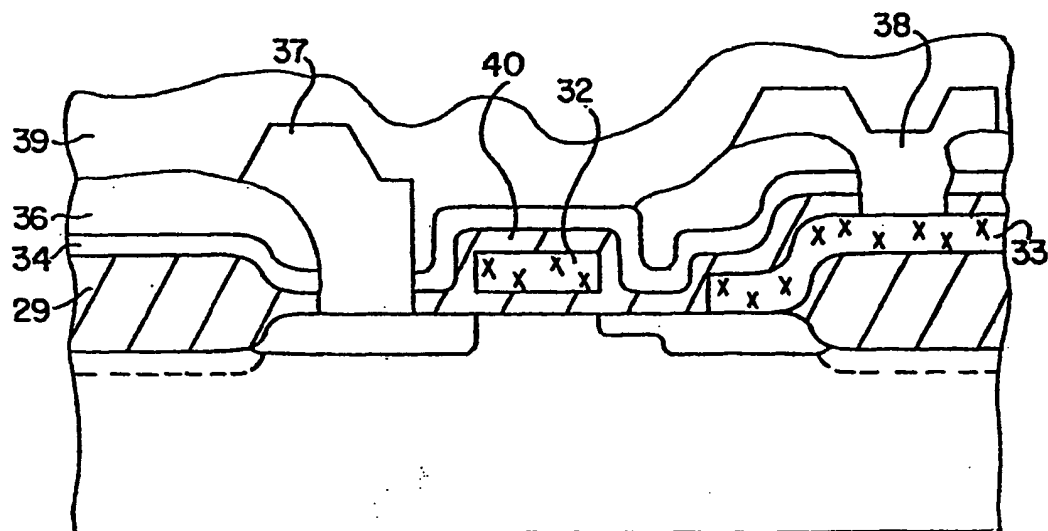


FIG. 21



European Patent
Office

EUROPEAN SEARCH REPORT

0132033
Application number

EP 84 30 3740

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
X	US-A-4 295 209 (W.B. DONLEY) * Claims 1,2; column 5, line 62 - column 6, line 61; figures 6-11 *	1-3,8, 10,13	H 01 L 21/82 H 01 L 27/10
X	US-A-4 364 167 (W.B. DONLEY) * Claims 1-3; column 5, line 63 - column 6, line 62; figures 6-11 *	1-3,8, 10,13	
A	US-A-4 273 303 (P.K.CHATTERJEE et al.) * Claims 1-17 *	1-4,7, 8,13	
A	US-A-4 364 165 (J.E. DICKMAN et al.) * Claims 3,4; column 7, lines 41-59 *	1,3,8, 13	
A	US-A-4 356 042 (J.M. GEDALY et al.) * Claims 1-4 *	1,3,8	H 01 L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 10-10-1984	Examiner ZOLLFRANK G.O.
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
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